Remarks

Reconsideration and withdrawal of the rejections set forth in the above-mentioned Official Action in view of the following remarks are respectfully requested.

Claims 1-19 are pending in the application, with Claims 1, 14 and 17 being independent. Claims 1, 14 and 17 have been amended and Claims 18 and 19 have been added herein.

Initially, as indicated in the previous response, Applicant is submitting herewith a submission of the sworn translation of the priority document.

Applicant notes with appreciation the indication that Claims 5, 6, 7/5-6, 8/5-6 and 9/7/5-6 recite allowable subject matter. These claims were objected to for being dependent upon rejected base claims. However, these claims will not be rewritten in independent form at this time because their respective independent claims are believed to be allowable for the reasons discussed below.

Claims 1-4, 7/1-4, 10-13 and 17 were rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 5,583,987 (Kobayashi et al.). Claims 8/1-4 and 9/7/1-4 were rejected under 35 U.S.C. § 103 as being unpatentable over Kobayashi et al. in view of U.S. Patent No. 5,929,672 (Mitani). Claims 14-16 were rejected under § 103 as being unpatentable over U.S. Patent No. 5,784,080 (Nitta et al.) in view of Kobayashi et al. These rejections are respectfully traversed.

As is recited in independent Claim 1, the present invention relates to an integrated-circuit apparatus including a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals and external clock signals. The circuit

blocks each respectively output an initialization completion signal for communicating completion of initialization after the circuit blocks are initialized. The CPU outputs an enable signal for permitting operations of the circuit blocks in accordance with the initialization completion signals output from the circuit blocks. The circuit blocks are permitted to perform the operations by the enable signal, the external reset signals and the external clock signals.

Independent Claim 14 is directed to an ink jet recording apparatus including an integrated-circuit apparatus for controlling recording using a recording head. The integrated-circuit apparatus is similar to that recited in independent Claim 1.

As recited in independent Claim 17, the present invention relates to a control method of an integrated-circuit apparatus having a CPU and a plurality of circuit blocks to be initialized in accordance with external reset signals and external clock signals. The method comprises the steps of initializing the circuit blocks, outputting an initialization completion signal for communicating completion of initialization in the initializing step, outputting an enable signal for permitting operations of the circuit blocks in accordance with the signal output in the initialization completion signal outputting step and permitting the circuit blocks to perform the operations by the enable signal, the external reset signals and the external clock signals.

The amended independent claims are supported in the original specification at least at the description at page 11, line 22 through page 12, line 11 and in Figs. 2 and 3. In particular, an enable signal 19 is output from a CPU 2 and if a reset signal is at H level, enable signals 21a, 21b are synchronized with a clock signal 5 and output to circuits 3 and

4. By such signals, circuits 3 and 4 become in an operation permitted state. Incidentally, support for newly-presented dependent Claims 18 and 19 can be found at least in Fig. 2, and in particular with regard to AND circuit 10a (10b) and F/F circuit 9b (9c).

With the above arrangement, an initialization process of a CPU at a circuit block can be executed at a proper timing.

Kobayashi et al. relates to initializing a multiprocessor system. As understood by Applicant, in the conventional information processing apparatus described therein, a plurality of CPUs 5a-5d receive a reset signal through line 23 and are reset or initialized as indicated in step H2 in Fig. 17. Reset signal 23 is cancelled, an initialization program is processed (H3) and then a master CPU executes a processor reset process to a slave CPU (H8). Slave CPUs 5b-5d report to master CPU 5a by initialization completion signal (H12). In other words, Applicant submits, master CPU 5a is not in a reset state. In Fig. 17 of Kobayashi et al., at step H2 and in col. 1, lines 55+, all CPUs 5a-5d are started by a reset signal indicated as disabled. However, no initialization timing is disclosed. Applicant submits that this is because each of the CPUs is independently capable of being started and the master CPU controls the slave CPUs to start a multiprocessor system by executing a reset process twice.

Thus, Applicant submits that Kobayashi et al. fails to disclose or suggest at least a CPU outputting an enable signal for permitting operations of circuit blocks in accordance with initialization completion signals output from the circuit blocks, and the circuit blocks being permitted to perform the operations by the enable signal, external reset signals and external clock signals, as is recited in independent Claims 1 and 14. Kobayashi

et al. also fails to disclose or suggest outputting an enable signal for permitting operations of circuit blocks in accordance with a signal output in an initialization completion signal outputting step, and permitting the circuit blocks to perform the operations by the enable signal, external reset signals and external clocks signals, as is recited in independent Claim 17.

Thus, Kobayashi et al. fails to disclose or suggest important features of the present invention recited in independent Claims 1, 14 and 17.

Mitani was cited by the Examiner for teaching power-on reset circuits for use in a one-chip microcomputer. Nitta et al. was cited by the Examiner for teaching a control apparatus for a serial printer. However, neither Mitani nor Nitta et al. is believed to remedy the deficiencies of Kobayashi et al. noted above with respect to the independent claims.

Thus, independent Claims 1, 14 and 17 are patentable over the citations of record. Reconsideration and withdrawal of the §§ 102 and 103 rejections are respectfully requested.

For the foregoing reasons, Applicant respectfully submits that the present invention is patentably defined by independent Claims 1, 14 and 17. Dependent Claims 2-13, 15, 16, 18 and 19 are also allowable, in their own right, for defining features of the present invention in addition to those recited in their respective independent claims. Individual consideration of the dependent claims is requested.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

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